Electronic Version
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Claims

[c1] 1.A trace-impedance-matched board comprising:
a substrate containing wiring traces that include an input trace ending at a first junction;
a plurality of branch traces on the substrate, the plurality of branch traces branching from the first junction to a plurality of endpoints;
wherein a first equivalent impedance is a reciprocal of a sum of reciprocals of branch impedances of branch traces branching from the first junction in the plurality of branch traces;
wherein an input impedance of the input trace is adjusted to match the first equivalent impedance.

[c2] 2.The trace-impedance-matched board of claim 1
wherein the input impedance is adjusted by enlarging a width of the input trace or a thickness of the input trace.

[c3] 3.The trace-impedance-matched board of claim 2
wherein a width of the input trace is matched to a sum of widths of branch traces branching from the first junction.

[c4] 4.The trace-impedance-matched board of claim 1

wherein each branch trace in the plurality of branch traces has an impedance within 10 percent of a base impedance Z0;
wherein the plurality of branch traces comprises N branch traces that branch form the first junction,
wherein N is a whole number of at least two;
wherein the input impedance is adjusted to be within 10 percent of Z0/N.

[c5] 5.The trace-impedance-matched board of claim 4 wherein input impedance of the input trace is adjusted by enlarging a width of the input trace;
wherein the input trace is N times wider than each of the branch traces in the plurality of branch traces.

[c6] 6.The trace-impedance-matched board of claim 5 wherein the trace-impedance-matched board is a memory module that further comprises dynamic-random-access memory (DRAM) chips mounted on the substrate;
wherein the plurality of branch traces have endpoints that are inputs to the DRAM chips.

[c7] 7.The trace-impedance-matched board of claim 6 wherein the DRAM chips are mounted on a first surface and on a second surface of the substrate;
wherein each branch trace drives an input of a first

DRAM chip mounted on the first surface and also drives an input of a second DRAM chip mounted on the second surface,

wherein the first DRAM chip and the second DRAM chip are mounted opposite each other with at least a partial overlap,

whereby branch traces drive pairs of DRAM chips mounted on opposite surfaces of the substrate.

[c8] 8.The trace-impedance-matched board of claim 7 wherein the input line is un-terminated and not connected to a termination resistor;

wherein each branch trace in the plurality of branch traces is un-terminated and not connected to a termination resistor;

whereby termination of the input line and branch traces is eliminated by trace-impedance-matching of the first junction.

[c9] 9.The trace-impedance-matched board of claim 2 further comprising:

a trunk branch trace branching from the first junction;

a second junction, receiving a signal driven from the input trace, through the first junction to the trunk branch trace; and

a plurality of secondary branch traces that branch from the second junction;

wherein the second junction outputs a signal to the plurality of secondary branch traces;
wherein a second equivalent impedance is a reciprocal of a sum of reciprocals of second branch impedances of secondary branch traces that branch from the second junction in the plurality of secondary branch traces;
wherein a trunk impedance of the trunk branch trace is adjusted to match the second equivalent impedance.

[c10] 10.The trace-impedance-matched board of claim 2 wherein the input trace carries a true signal of a differential signal;
further comprising:
a complement input trace ending at a complement junction, the complement input trace carrying a complement signal of the differential signal;
a plurality of complement branch traces on the substrate, the plurality of complement branch traces branching from the complement junction to a plurality of complement endpoints;
wherein a first complement equivalent impedance is a reciprocal of a sum of reciprocals of complement branch impedances of complement branch traces branching from the complement junction in the plurality of complement branch traces;
wherein a complement input impedance of the comple-

ment input trace is adjusted to match the first complement equivalent impedance,
whereby the differential signal is carried by a pair of impedance-matched traces.

[c11] 11.An impedance-matched module comprising:
a substrate having chips mounted thereon;
a plurality of wiring traces formed within or on the substrate;
an input line in the plurality of wiring traces;
a first branch line in the plurality of wiring traces;
a second branch line in the plurality of wiring traces;
a third branch line in the plurality of wiring traces;
a primary junction connecting an end of the input line to the first branch line, the second branch line, and to the third branch line;
wherein a first equivalent impedance is a parallel combination of impedances of branches from the primary junction including a first impedance of the first branch line, a second impedance of the second branch line, and a third impedance of the third branch line;
wherein the input line has an input impedance that is matched to the first equivalent impedance by widening or thickening the input line.

[c12] 12.The impedance-matched module of claim 11 wherein the first branch line drives an input of a first chip

mounted on the substrate;
wherein the second branch line drives an input of a second chip mounted on the substrate;
wherein the third branch line drives an input of a third chip mounted on the substrate.

[c13] 13.The impedance-matched module of claim 11 wherein the input line, and the first, second, and third branch lines are not connected to terminating resistors.

[c14] 14.The impedance-matched module of claim 13 wherein the input line has the input impedance that is matched to within 20-percent of the first equivalent impedance.

[c15] 15.The impedance-matched module of claim 14 further comprising:
a complement input line in the plurality of wiring traces;
a complement first branch line in the plurality of wiring traces;
a complement second branch line in the plurality of wiring traces;
a complement third branch line in the plurality of wiring traces;
a complement primary junction connecting an end of the complement input line to the complement first branch line, the complement second branch line, and to the complement third branch line;

wherein a second equivalent impedance is a parallel combination of impedances of branches from the complement primary junction including a fourth impedance of the complement first branch line, a fifth impedance of the complement second branch line, and a sixth impedance of the complement third branch line;
wherein the complement input line has an impedance that is matched to the second equivalent impedance by widening or thickening the complement input line;
wherein the input line and the complement input line receive a differential signal.

[c16] 16.The impedance-matched module of claim 15 wherein input line and the complement input line receive a differential clock to the chips mounted on the substrate.

[c17] 17.A module with impedance-matched trace junctions comprising:
substrate means for supporting chips driven by wiring traces formed on the substrate means;
input interconnect means for transmitting a signal along a wiring trace to a first junction;
first branch interconnect means for connecting the signal to a first chip on the substrate means;
second branch interconnect means for connecting the signal to a second chip on the substrate means; and
first junction means, receiving the signal from the input

interconnect means, for connecting the signal to the first branch interconnect means and to the second branch interconnect means, the first junction means being a junction of the wiring traces;
wherein an input impedance of the input interconnect means matches an equivalent impedance of branch traces driven from the first junction means, including the first and second branch interconnect means,
whereby impedance is matched at the first junction means.

[c18] 18.The module with impedance-matched trace junctions of claim 17 wherein the input impedance is matched to within 20-percent of the equivalent impedance.

[c19] 19.The module with impedance-matched trace junctions of claim 18 wherein a width of the input interconnect means is matched to a sum of widths of branch traces driven from the first junction means, including a first width of the first branch interconnect means and a second width of second branch interconnect means.

[c20] 20.The module with impedance-matched trace junctions of claim 17 further comprising:
first trunk interconnect means for further distributing the signal from the first junction means, the first trunk interconnect means being a branch trace from the first

junction means;

third branch interconnect means for connecting the signal to a third chip on the substrate means;

fourth branch interconnect means for connecting the signal to a fourth chip on the substrate means; and

second junction means, receiving the signal from the first trunk interconnect means, for connecting the signal to the third branch interconnect means and to the fourth branch interconnect means, the second junction means being another junction of the wiring traces;

wherein a trunk impedance of the first trunk interconnect means matches a secondary equivalent impedance of secondary branch traces driven from the second junction means, including the third and fourth branch interconnect means,

whereby impedance is matched at the second junction means.